

Stability Analysis Tool User's Guide

For use with Board Mounted
DC-DC converters

V1.3

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1

Introduction

The Stability Analysis Tool (SAT) is a Microsoft Excel-based program that provides a Bode plot of the voltage loop gain of a DC-DC converter for a variety of external loads. From this plot, information such as crossover frequency and gain and phase margins can be obtained.

In classical control theory, the stability of a feedback system is assessed by evaluating its gain and phase margin which are read directly from the Bode plot of the loop gain. The loop gain of a DC-DC converter depends not only on the converter characteristics but also on the load characteristics and the output voltage sense location. This dependence of loop gain on load and sense location makes it impossible for the power converter manufacturer to determine stability margins in an actual application, since the load (especially the number, type and location of output bulk capacitors, parasitic inductances, etc.) and the output voltage sense location are unknown. Due to this, in the past if the customer wanted to determine stability margins, the loop gain would have to be measured using a breadboard of the power-supply and the load network using a network analyzer.

The Stability Analysis Tool decouples the combined converter+load system into two subsystems; one representing the converter and the other representing the load. Tyco Electronics Power Systems provides converter data files on its web site. The customer can download the converter data file and import it into the SAT. SAT allows choosing one of five different configurations to best represent the combination of load representation and voltage sense location. The tool then allows assessment of the stability characteristics without the user having to build a prototype of the power supply and the load network and avoids making measurements.

System Requirements

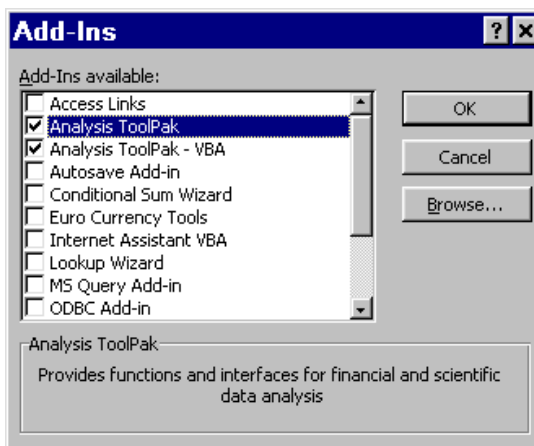
SAT v1.3 runs under the following systems:

- 1)** Windows 95, 98, 2000 or Windows NT version 4 operating systems
- 2)** Microsoft Excel 97 SR-2 or Excel 2000
- 3)** Intel Pentium® class or above processor and at least 64 MB of RAM

Installation and Usage

You should first read and accept the terms of the SAT usage.

- Download the file SAT_v1.3.xls from the Tyco Electronics Power Systems web site (given below) to a directory on your computer.
- Download one or more module data file(s) to the same directory.
- You can start up the tool by following the usual procedures to open an Excel Worksheet and follow the directions on the screen. Make sure that the Analysis Toolpak Add-ins are enabled in Excel. Go to **Tools** menu in Excel and click on **Add-Ins**. Check (tick) on **Analysis Toolpack** and **Analysis Toolpack – VBA**.



Technical Support

For technical support, please contact us at

USA **Tyco Electronics Power Systems**
3000 Skyline Drive
Mesquite, TX 75149
USA

Phone - 800-526-7819
Fax - 888-315-5182

Outside

U.S.A.: Refer to our Web site below for Service and Support in other regions of the world

Web: <http://power.tycoelectronics.com/>

Using SAT

When you start SAT, you will see the window shown in Figure 1.

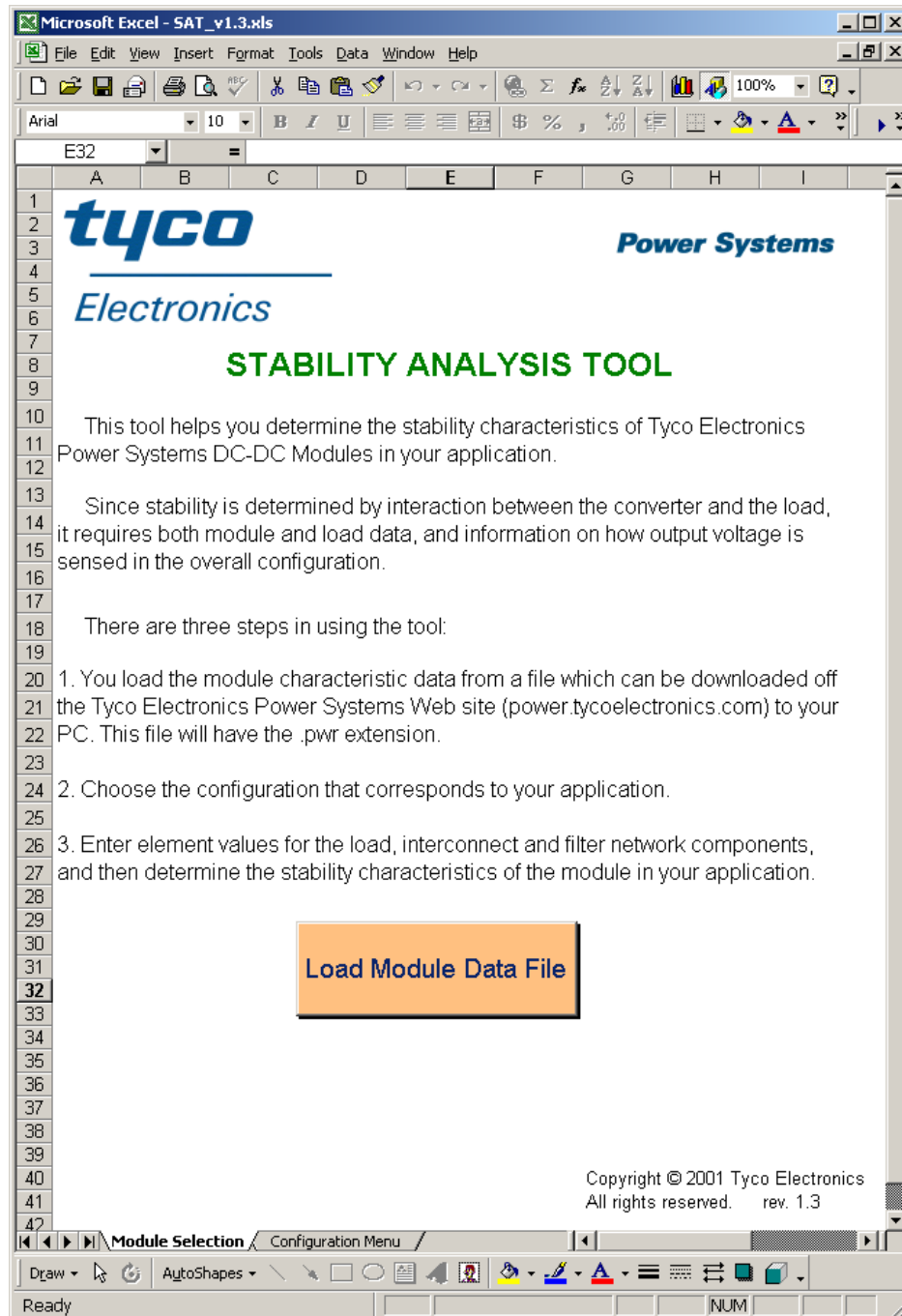



Fig. 1. SAT Introduction and Module Selection page

- There are two sheets, "*Module Selection*" and "*Configuration Menu*" shown initially at the bottom left-hand section of the Excel spreadsheet. Each session should start at the "*Module Selection*" sheet.
- Click on the button  This will bring the module data file import window as shown below in Figure 2.

Note that all module data files have .pwr extensions. If you have not already downloaded the module data files for the particular modules you wish to analyze, they will need to be downloaded before you can use the tool.

- Choose the module that you want to use in your application by selecting the corresponding module data file. In this guide, we will use the JFW050A module as an example.
- After highlighting the JFW050A.pwr file, click on the "OK" button or hit "ENTER". SAT will load the module data file and move to the *Configuration Menu* as shown in Figure 3. You may want to save SAT_v1.3.xls file under a different name so that the original one that you downloaded remains unchanged.

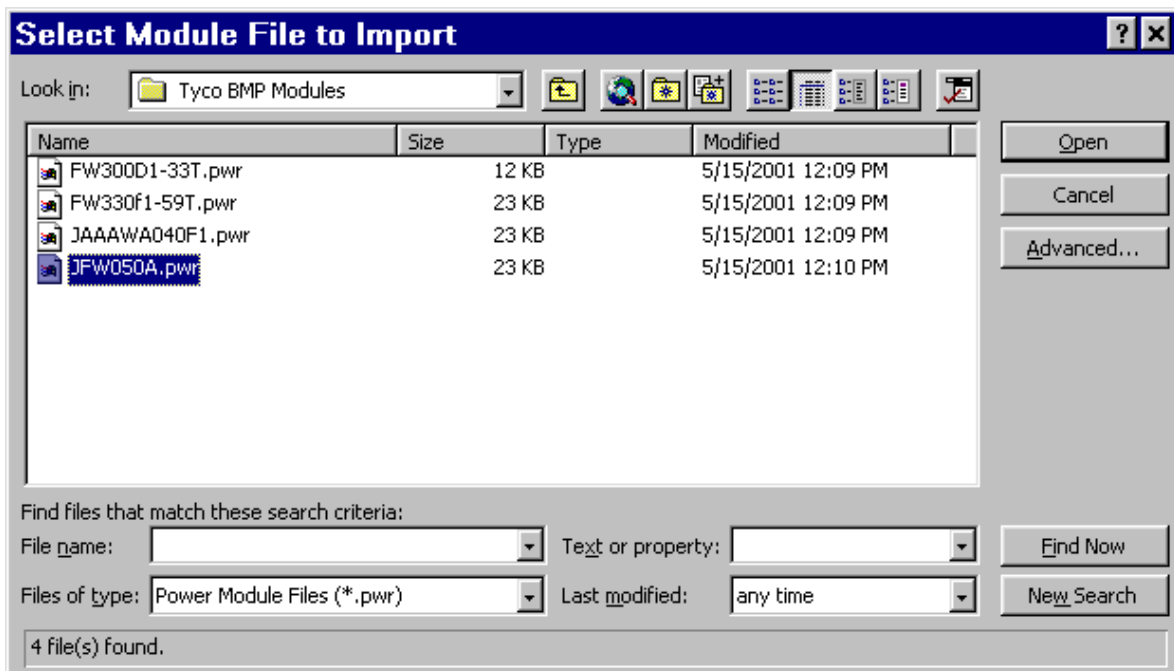


Fig. 2. Module data file import window

- If you want to choose a different module data file, you can always go back to the *Module Selection* sheet to change it.
- The *Configuration Menu* lists five choices for representing the load circuit topology.
 - The first configuration is a simple one where the output voltage is sensed directly at the output pins of the module. The capacitor is modeled as a series combination of equivalent series resistance (ESR) and equivalent series inductance (ESL). If all the capacitors are the same type (e.g. aluminum electrolytic) and capacitance value (e.g. 6800 μ F), then this is a reasonable

Configuration Menu

Please click on the appropriate box to choose the configuration for your application

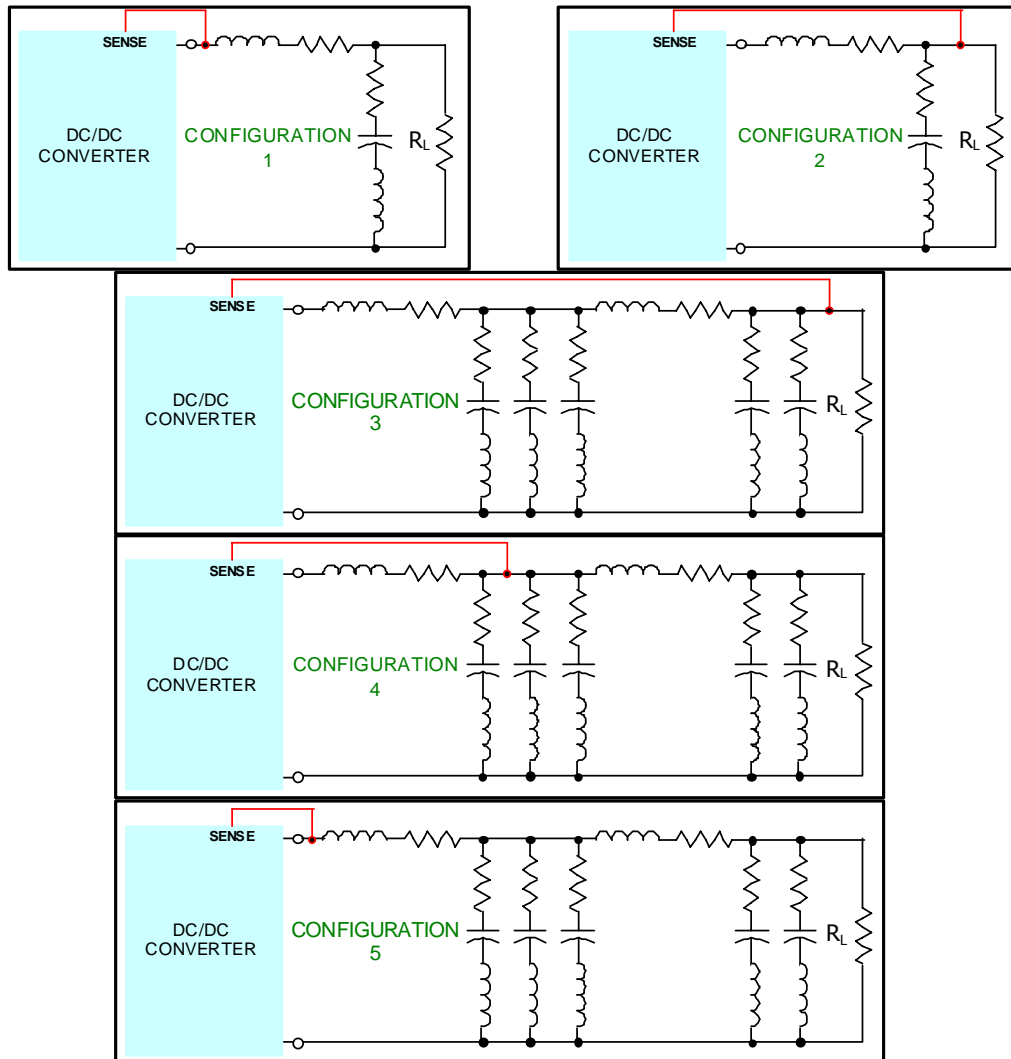


Fig. 3. Circuit configuration

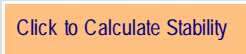
model of the capacitor bank. The load is modeled by the resistance R_L .

- The second configuration is similar to the first one except that the voltage sense location is moved from the output pins of the module to the load. In this case, the voltage sensed and regulated is not the module output voltage but the voltage across the load, a situation commonly referred to as "*remote sensing*".
- The remaining three configurations (3, 4 and 5) allow the inclusion of more detailed models of the capacitor banks and parasitic elements between the module and the load. In some applications, the power module is mounted on a separate printed circuit board and supplies a number of loads on different PCBs. In this case, it is common to have one capacitor bank on the power board and another one on the load board.

The first capacitor bank, which is a parallel combination of three capacitors, is usually located as close as possible to the module output pins. It conveniently allows for modeling different types of capacitors such as aluminum and tantalum electrolytics and ceramics. When the size and type of capacitors used in a bank are different, their individual frequency responses vary greatly from one another and hence they cannot be modeled as a lumped capacitor as shown in the first two configurations. Note that if you only have one or two types of capacitors, you can still use the model by setting the values corresponding to the other capacitor to zero.

The second capacitor bank is typically placed as close as possible across the load terminals to improve dynamic response during load transients by minimizing the voltage overshoot and undershoot. The capability of modeling two capacitors with their ESR and ESL are provided to model different types and sizes of capacitors.

The three configurations also allow for modeling various sense points for the feedback voltage. Feedback voltage can be sensed across the load (case 3), across the capacitor bank (case 2), or across the module output.

- Click on the configuration picture suitable for your application. In this example, we will choose Configuration 4. Clicking on the picture will bring that configuration's page as shown in Figure 4.
- The top left section shows the configuration circuit with the feedback voltage sense path depicted in red. Underneath the configuration circuit diagram, circuit parameters are listed with default values that can be edited in blue. The JFW050A module is a 5V, 10A output module and hence in this example, the load resistance is set at 0.5 ohms, indicating a 10A load. You should set the load resistance value corresponding to the actual load in your application. The resistors R_{a1} , through R_{a3} , and R_{b1} through R_{b3} are the ESRs of the capacitors and the inductances L_{a1} through L_{b3} are the ESLs.
- Enter all circuit parameters of your application. When you finish editing the parameter values, click on the  button.

SAT draws the Bode plot of the voltage loop gain on the right half of the page as shown in Figure 5. The phase margin, which is a measure of stability, and the gain crossover frequency, which is a measure of fast transient response, are also calculated and presented below the Bode plot.

You can enter your notes under the "Notepad Area for JFW050A Module" section in the left lower corner of the page. You can also edit the circuit parameters and simulate various what-if scenarios and record the results on the same page. Figure 6 below compares two scenarios where the value of C_{b2} is changed from 1000 μF to 6800 μF .

- To investigate a different configuration, click on the *Configuration Menu* tab at the bottom of the Excel worksheet which will take you back to the configuration-selection page. If you click on the circuit diagram for Configuration 2, the page for that configuration will appear in the window and the Configuration 4 page will disappear (Figure 7). You can now repeat the analysis in a manner similar to the previous case. There is no need to re-load the module data file for JFW050A to perform an analysis for another configuration.

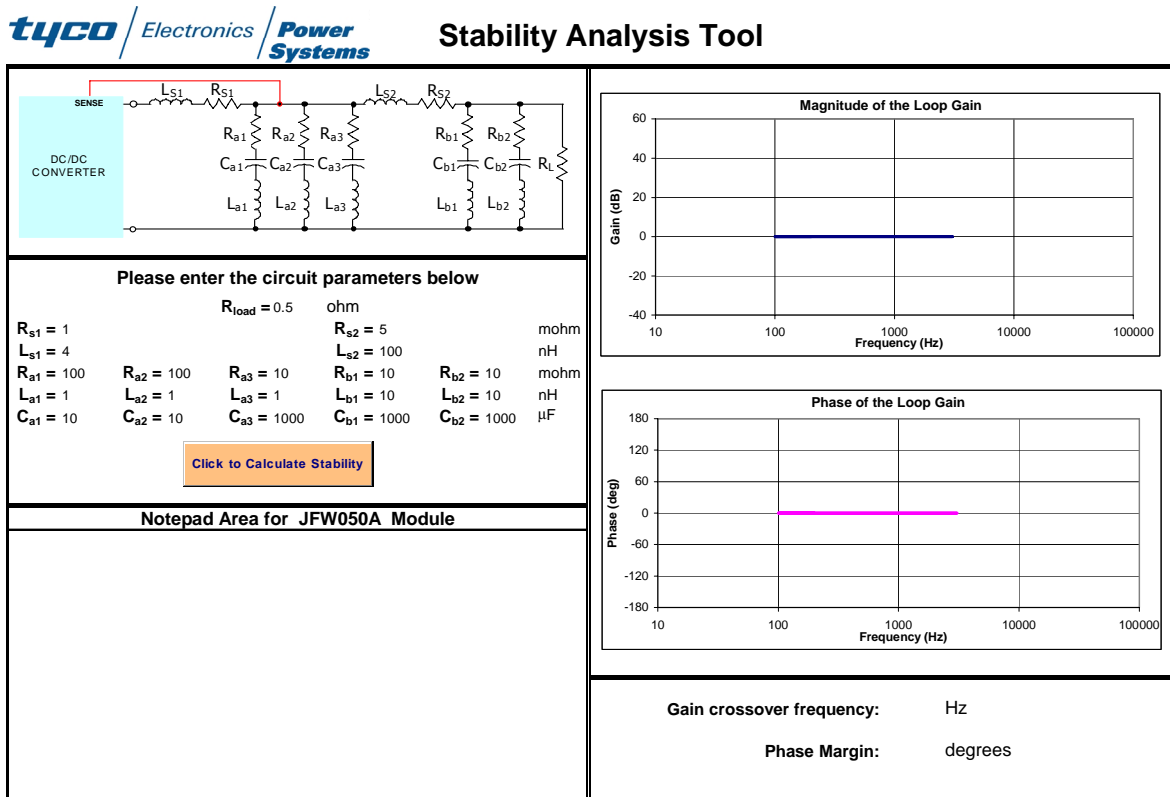


Fig. 4. Page for entering and editing circuit parameters, shown for the case of configuration 4.

Stability Analysis Tool

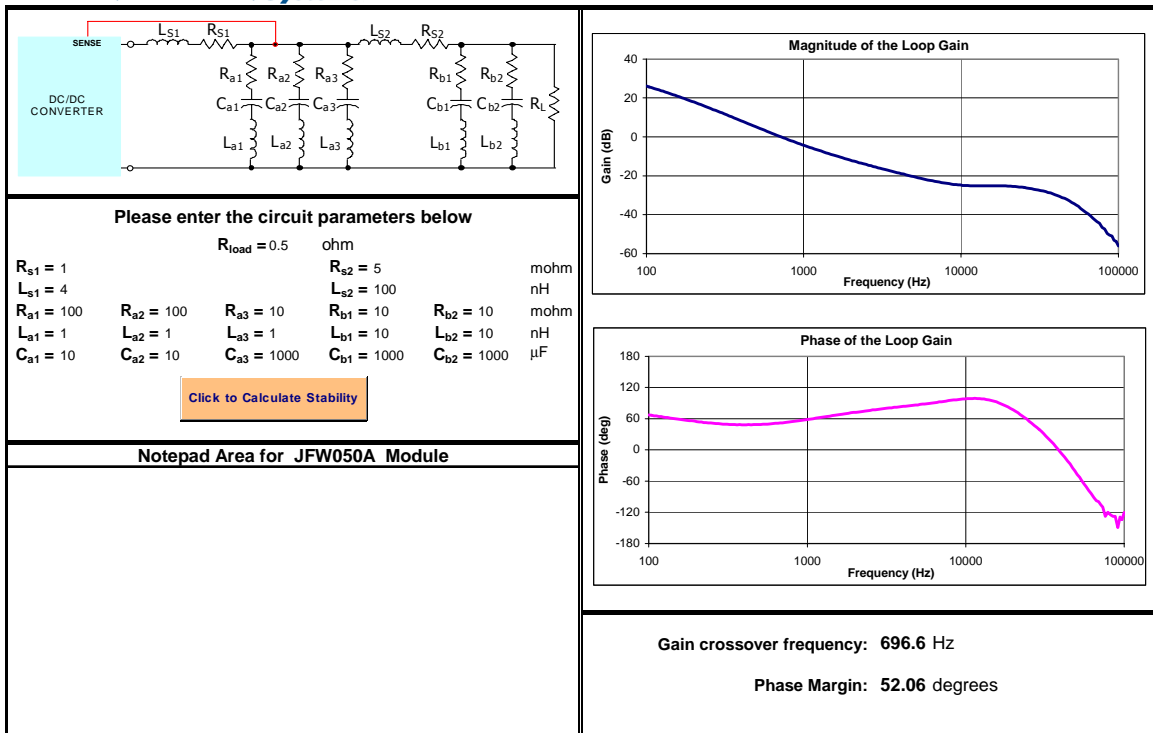


Fig. 5. Voltage-loop-response Bode plot with phase margin and gain crossover frequency calculated and displayed.

Stability Analysis Tool

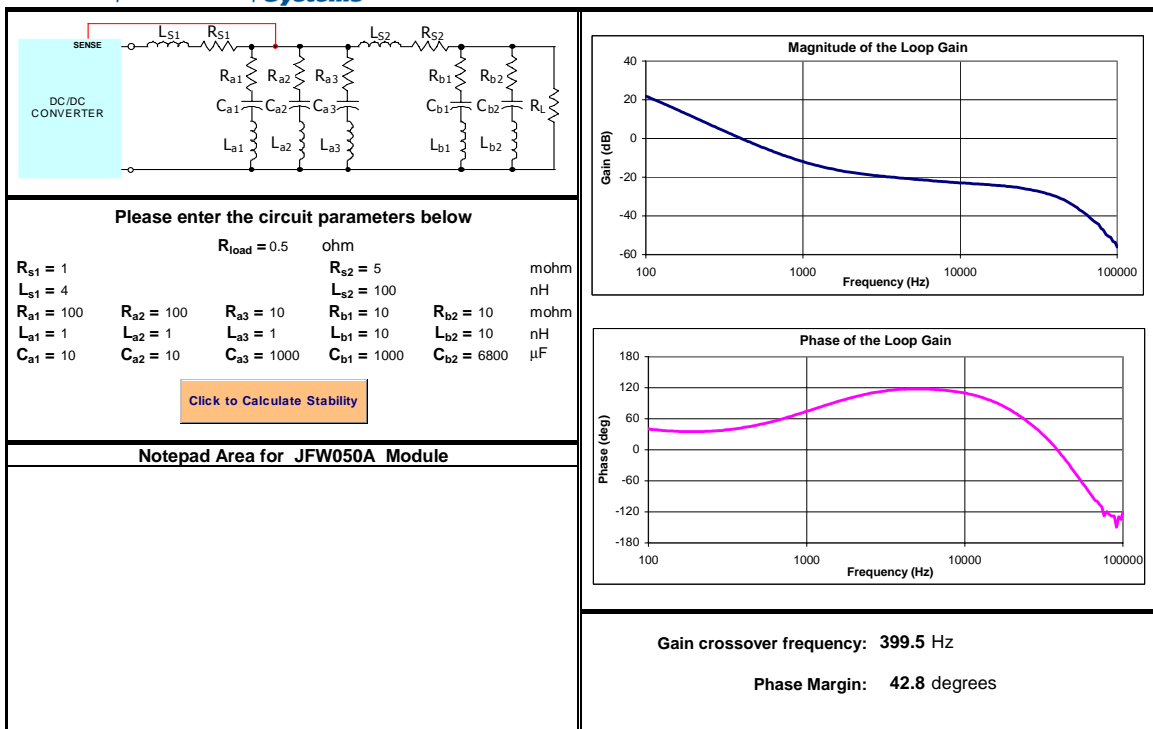


Fig. 6. Voltage loop response Bode plot when $C_{b2}=6800 \mu$ F

- To analyze a different module, you should select the *Module Selection* tab at the bottom of the Excel Worksheet to go back to the first page and load the data file for the new module. Note that the new data file will overwrite the old one belonging to the JFW050A. If you want to keep your analysis results for the JFW050A module, you should save SAT_v1.3.xls under a different name, e.g. JFW050A.xls.

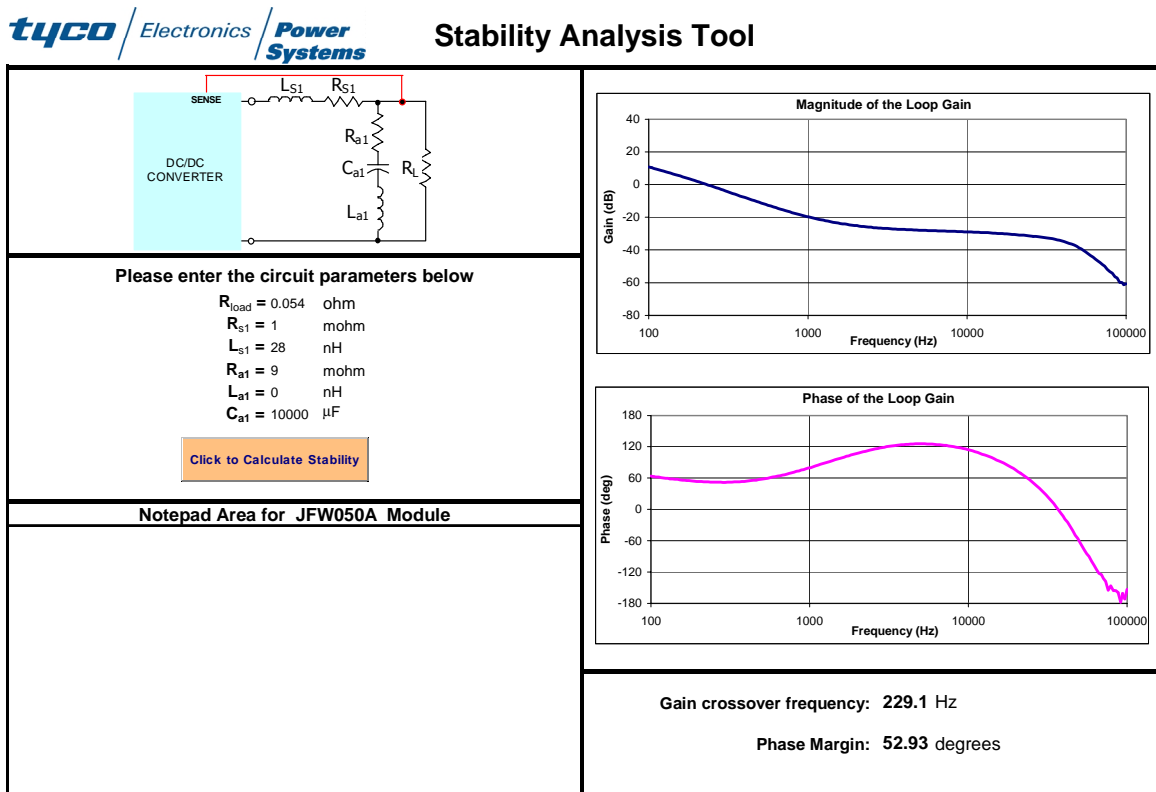


Fig. 7. Stability analysis of the JFW050A for Configuration 2.

Paralleled Modules

Paralleled modules can also be analyzed using SAT. Typically, in systems with paralleled modules, active current sharing is used to distribute the stresses evenly between modules. As described in [1], such a system can be analyzed separately for common-mode stability (which is solely dependent on the number of modules, the characteristics of the modules and the load), and differential-mode stability (which only depends on the current-sharing loop and is independent of the number of modules paralleled or the load). Since differential-mode stability is independent of the load, the manufacturer of the module is able to ensure that the current-sharing loop is stable. However, common-mode stability depends both on the number of modules paralleled and the load, both of which are controlled by the

customer application.

SAT can be used to assess the common-mode stability characteristics of a paralleled converter system by analyzing an equivalent single-module system. The single-module equivalent is obtained by scaling the load by the number of paralleled modules. For example, in a two module parallel system, the load is scaled by a factor of two by doubling the load resistance, ESR's and ESLs, and reducing the capacitances by half. The results from SAT are then valid for the paralleled converter system as well

This method assumes that the layout is symmetrical in the sense that all parasitic impedances between the modules and the load are substantially equal and the sense locations of all modules are the same. If there is any discrepancy, then the single equivalent module approach will yield a different answer than the actual paralleled system.

References

- [1] V. Joseph Thottuvelil, George C. Verghese, "Analysis and Control Design of Paralleled DC/DC Converters with Current Sharing", IEEE Trans. On Power Electronics, July 1998, pp. 635-644.
- [2] Cahit Gezgin, Wayne C. Bowman, V. Joseph Thottuvelil, "A Stability Analysis Tool for DC-DC Converters", IEEE Applied Power Electronics Conference 2002, vol.1, pp. 367-373.

3

Limitations of SAT

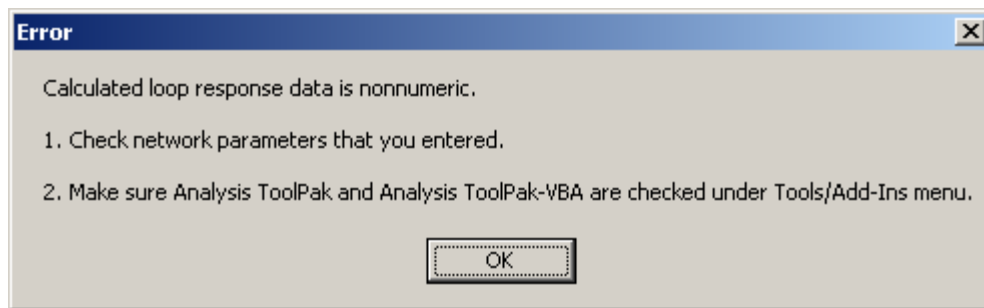
Although SAT is a powerful tool, please keep in mind the following :

1. The loop gain Bode plot and phase margin predicted by SAT are valid when the module is operating in continuous conduction mode (CCM). Therefore, make sure that R_L is sufficiently low enough to guarantee a load current that leads to CCM operation. Modules with synchronous rectifier based output stages operate in CCM throughout the entire load current range.
2. It is assumed that the module input voltage is at the nominal value, e.g. 48V for xWxxx, 24V for xCxx modules, etc. The loop response and phase margin will be different if the input voltage is not at the nominal value. However, for stability assessment purposes, since there are usually requirements for margins of $>45^\circ$ and 12dB, performing a stability analysis at nominal voltage of 48V is typically sufficient.
3. For buck derived converter topologies, the sensitivity of voltage loop response on load variations is small. Therefore, SAT captures the loop response over load variations, from CCM limit to full load, with reasonable accuracy. Future releases of SAT will address the effect of input voltage variations on the stability margins.

4

Troubleshooting

If you encounter the following message when running SAT,



there are two possibilities for the error message.

1. Some of the parameters you entered for your network are nonnumeric.
2. You have not enabled the Analysis Toolpack and Analysis Toolpack – VBA in your Excel environment as described in page 5 of this document under “Installation and Usage”. If you cannot see Analysis Toolpack and Analysis Toolpack – VBA under the Tools/AddIns tab in Excel, then you have to reinstall Excel with those options checked during installation.

Make sure that you have the correct Excel settings and numeric data for the network parameters.